Electronic Version
Stylesheet Version v1.1.1

Claims

[c1] What is claimed is:

1. A method of forming a varactor, the method comprising:

providing a substrate, the substrate comprising an ion well of a first conductivity type and a plurality of isolation structures positioned on the ion well, the isolation structures defining at least an active area on the ion well;

implanting ions of the first conductivity type into the ion well to form a doping region within the active area;

forming a doping layer of a second conductivity type on the substrate to cover portions of the doping region; and

forming a salicide layer on the doping region and the doping layer.

[c2] 2. The method of claim 1 further comprising forming a salicide block on the doping layer to prevent a junction between the doping region and the doping layer from being destroyed by the salicide layer.

[c3] 3. The method of claim 1 wherein the substrate comprises at least a buried doping region of the first conductivity type positioned beneath the ion well.

[c4] 4. The method of claim 1 wherein the substrate comprises at least a CMOS transistor, and the doping region of the varactor and a lightly doped drain of the CMOS transistor are formed using the same doping process.

[c5] 5. The method of claim 4 wherein before forming the doping layer, the method further comprises forming at least a protective layer on the substrate to cover the CMOS transistor.

[c6] 6. The method of claim 1 wherein the doping layer comprises an epitaxial layer.

[c7] 7. The method of claim 1 wherein the doping layer comprises a polysilicon layer.

[c8] 8. The method of claim 1 further comprising an ion implantation process to implant ions of the second conductivity type into the doping layer to adjust the resistance of the doping layer.

[c9] 9. The method of claim 1 wherein a doping concentration of the doping region is higher than a doping concentration of the ion well.

[c10] 10. A method of forming at least a CMOS transistor and at least a varactor on a substrate, the substrate comprising a first region for forming the CMOS transistor and a

second region for forming the varactor, the method comprising:

implanting ions of a first conductivity type into the substrate to form at least a first ion well in the first region and at least a second ion well in the second region;

implanting ions of a second conductivity type into the substrate to form at least a third ion well in the first region;

forming a plurality of isolation structures on the substrate;

forming a first gate on the first ion well and a second gate on the third ion well;

implanting ions of the first conductivity type into the substrate to form two first lightly doped drains on the third ion well, and simultaneously form a doping region on the second ion well;

implanting ions of the second conductivity type into the substrate to form two second lightly doped drains on the first ion well;

forming a spacer on both sides of the first gate and on both sides of the second gate;

forming two first source/drain regions of the second conductivity type on the first ion well, and forming two second source/drain regions of the first conductivity type on the third ion well;

forming a protective layer on the substrate, the protec-

tive layer comprising an opening to expose the doping region;

forming a doping layer of the second conductivity type on doping region; and

performing a salicidation process to form a salicide layer on the substrate.

[c11] 11. The method of claim 10further comprising forming a salicide block on the doping layer to prevent a junction between the doping region and the doping layer from being destroyed by the salicide layer.

[c12] 12. The method of claim 10 further comprising forming at least a buried doping region of the first conductivity type beneath the first ion well and the second ion well.

[c13] 13. The method of claim 10 wherein the doping layer comprises an epitaxial layer.

[c14] 14. The method of claim 10 wherein the doping layer comprises a polysilicon layer.

[c15] 15. The method of claim 10 further comprising an ion implantation process to implant ions of the second conductivity type into the doping layer to adjust the resistance of the doping layer.

[c16] 16. The method of claim 10 wherein a doping concen-

tration of the doping region is higher than a doping concentration of the second ion well.